

Features

- AEC-Q100 with extended temperature range (-40°C to 105°C)
- Any frequency between 220.000001 MHz and 725 MHz, accurate to 6 decimal places. For frequency between 1 and 220 MHz, see [SiT9386](#)
- LVPECL, LVDS and HCSL output signaling
- Frequency stability as low as ± 25 ppm – contact [SiTime](#)
- 0.23 ps RMS (typ) phase jitter (random, 12 kHz to 20 MHz)
- Industry-standard packages: 3.2 x 2.5, 7.0 x 5.0 mm
- Contact [SiTime](#) for 5.0 x 3.2 mm package

Applications

- 100 Gbps Ethernet, SONET, SATA, SAS, Fibre Channel
- Telecom, networking, instrumentation, storage, servers

INSTANT
SAMPLESSEARCH
INVENTORYGREEN
SOLUTIONSLIFETIME
WARRANTY

Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination show in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Table 1. Electrical Characteristics – Common to LVPECL, LVDS and HCSL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	220.000001	–	725	MHz	Accurate to 6 decimal places
Frequency Stability						
Frequency Stability		-25	–	+25	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations. Contact SiTime for ± 25 ppm.
		-50	–	+50	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations.
First Year Aging	F_aging1	–	± 1	–	ppm	At 25°C
Temperature Range						
Operating Temperature Range	T_use	-40	–	+85	°C	Industrial
		-40	–	+105	°C	Extended Industrial
Supply Voltage						
Supply Voltage	Vdd	2.97	3.30	3.63	V	
		2.70	3.00	3.30	V	
		2.52	2.80	3.08	V	
		2.25	2.50	2.75	V	
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE
Input Pull-up Impedance	Z_in	–	100	–	k Ω	Pin 1, OE logic high or logic low
Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Startup and OE Timing						
Startup Time	T_start	–	–	3.0	ms	Measured from the time Vdd reaches its rated minimum value.
OE Enable/Disable Time	T_oe	–	3.8		μ s	f = 322.265652 MHz

Table 2. Electrical Characteristics – LVPECL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	I _{dd}	–	–	94	mA	Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V
OE Disable Supply Current	I _{OE}	–	–	63	mA	OE = Low
Output Disable Leakage Current	I _{leak}	–	0.15	–	μA	OE = Low
Maximum Output Current	I _{driver}	–	–	32	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	V _{dd} -1.1	–	V _{dd} -0.7	V	
Output Low Voltage	VOL	V _{dd} -1.9	–	V _{dd} -1.5	V	
Output Differential Voltage Swing	V _{Swing}	1.2	1.6	2.0	V	See Figure 3
Rise/Fall Time	T _r , T _f	–	225		ps	20% to 80%
Jitter						
RMS Phase Jitter (random)	T _{phj}		0.225		ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, Includes spurs. 7.0 x 5.0 mm package.
		–	0.225		ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, Includes spurs. 3.2 x 2.5 mm package.
		–	0.1		ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, Includes spurs, all V _{dd} levels
RMS Period Jitter ^[1]	T _{jitt}	–	1.0		ps	f = 322.265625 MHz, V _{dd} = 3.3V or 2.5V

Notes:

1. Measured according to JESD65B

Table 3. Electrical Characteristics – LVDS Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	I _{dd}	–	–	89	mA	Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V
OE Disable Supply Current	I _{OE}	–	–	67	mA	OE = Low
Output Disable Leakage Current	I _{leak}	–	0.15	–	μA	OE = Low
Output Characteristics						
Differential Output Voltage	VOD	250	–	455	mV	See Figure 4
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 4
Offset Voltage	VOS	1.125	–	1.375	V	See Figure 4
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 4
Rise/Fall Time	T _r , T _f	–	370		ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 4
Jitter						
RMS Phase Jitter (random)	T _{phj}	–	0.215		ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, Includes spurs. 7.0 x 5.0 mm package.
		–	0.235		ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, Includes spurs. 3.2 x 2.5 mm package.
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, Includes spurs, all V _{dd} levels
RMS Period Jitter ^[2]	T _{jitt}	–	0.92		ps	f = 322.265625 MHz, V _{dd} = 3.3V or 2.5V

Notes:

2. Measured according to JESD65B

Table 4. Electrical Characteristics – HCSL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	I _{dd}	–	–	97	mA	Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V
OE Disable Supply Current	I _{OE}	–	–	63	mA	OE = Low
Output Disable Leakage Current	I _{leak}	–	0.15	–	μA	OE = Low
Maximum Output Current	I _{driver}	–	–	35	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	0.60	–	0.90	V	See Figure 2
Output Low Voltage	VOL	-0.05	–	0.08	V	See Figure 2
Output Differential Voltage Swing	V _{Swing}	1.2	1.4	1.9	V	See Figure 3
Rise/Fall Time	Tr, Tf	–	360		ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 2
Jitter						
RMS Phase Jitter (random)	T _{phj}	–	0.215		ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, Includes spurs. 7.0 x 5.0 mm package.
		–	0.235		ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, Includes spurs. 3.2 x 2.5 mm package.
		–	0.1		ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, Includes spurs, all V _{dd} levels
RMS Period Jitter ^[3]	T _{jitt}	–	0.92		ps	f = 322.265625 MHz, V _{dd} = 3.3V or 2.5V

Notes:

- 3. Measured according to JESD65

Table 5. Pin Description

Pin	Map		Functionality
1	OE/NC	Output Enable (OE)	H ^[4] : specified frequency output L: output is high impedance
		Non Connect (NC)	H or L or Open: No effect on output frequency or other device functions
2	NC	NA	No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	V _{dd} Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	V _{dd}	Power	Power supply voltage ^[5]

Notes:

- 4. In OE mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
- 5. A capacitor of value 0.1 μF or higher between V_{dd} and GND is required. An additional 10 μF capacitor between V_{dd} and GND is required for the best phase jitter performance

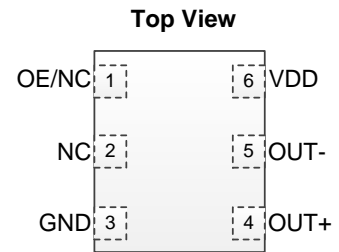


Figure 1. Pin Assignments

Table 6. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Vdd	-0.5	4.0	V
VIH		Vdd + 0.3V	V
VIL	-0.3		V
Storage Temperature	-65	150	°C
Maximum Junction Temperature		130	°C
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C

Table 7. Thermal Considerations^[6]

Package	θ_{JA} , 4 Layer Board (°C/W)	θ_{JC} , Bottom (°C/W)
3225, 6-pin	80	30
7050, 6-pin	52	19

Notes:

6. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

Table 8. Maximum Operating Junction Temperature^[7]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	95°C
85°C	110°C
105°C	–

Notes:

7. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 9. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	<i>g</i>
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	<i>g</i>
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

Waveform Diagrams

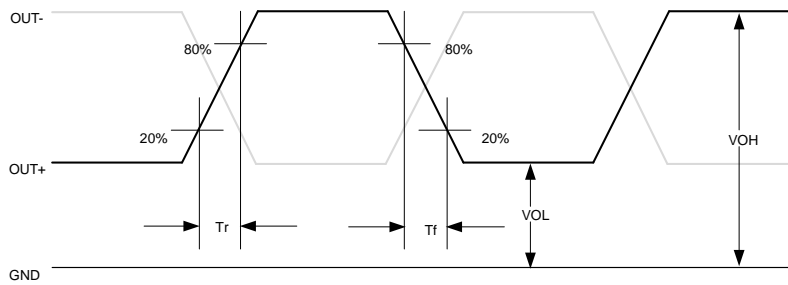


Figure 2. LVPECL/HCSL Voltage Levels per Differential Pin (OUT+/OUT-)

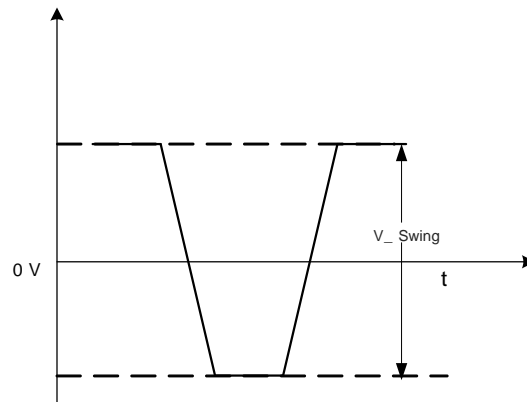


Figure 3. LVPECL/HCSL Voltage Levels across Differential Pair

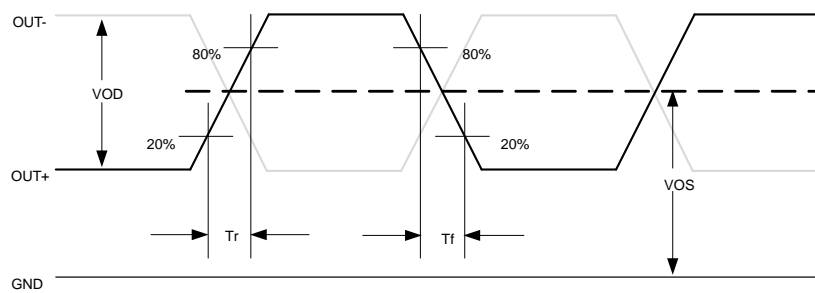


Figure 4. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

Termination Diagrams

LVPECL:

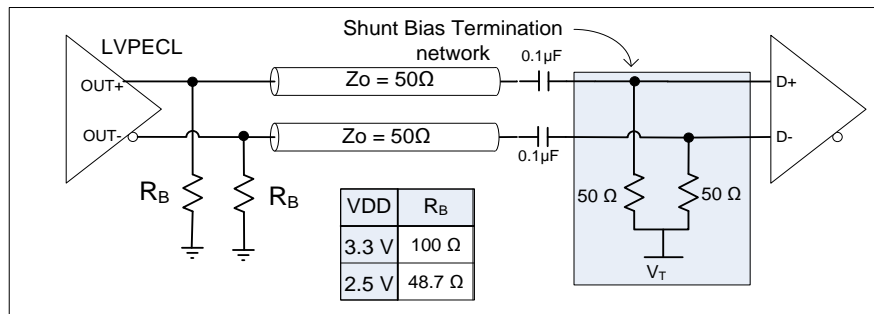


Figure 5. LVPECL with AC-coupled termination

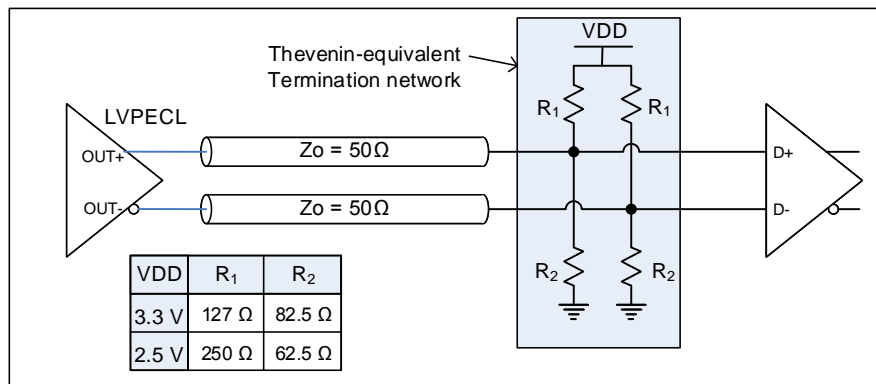


Figure 6. LVPECL DC-coupled load termination with Thevenin equivalent network

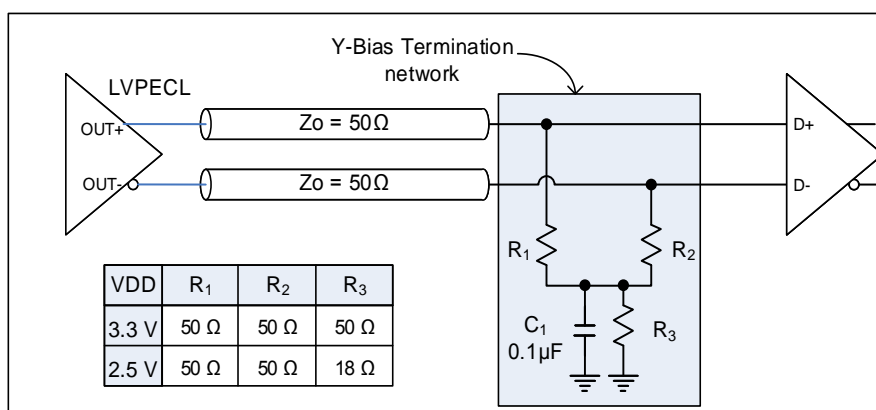


Figure 7. LVPECL with Y-Bias termination

Termination Diagrams (Continued)

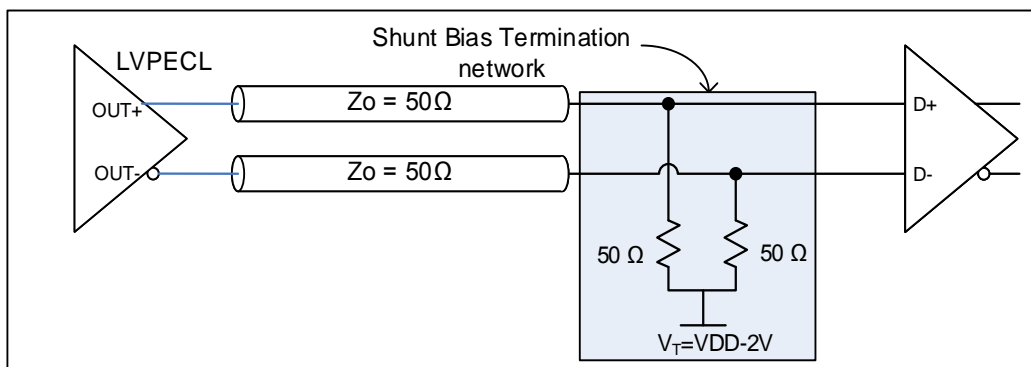


Figure 8. LVPECL with DC-coupled parallel shunt load termination

Termination Diagrams (Continued)

LVDS:

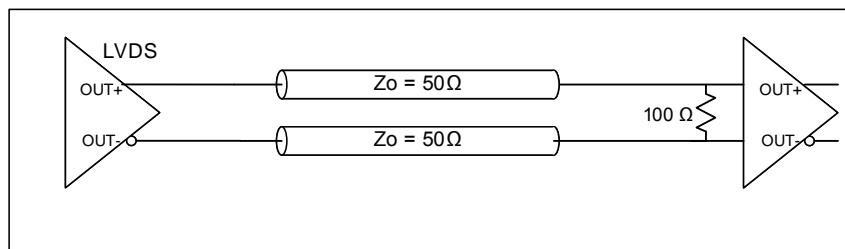


Figure 9. LVDS single DC termination at the load

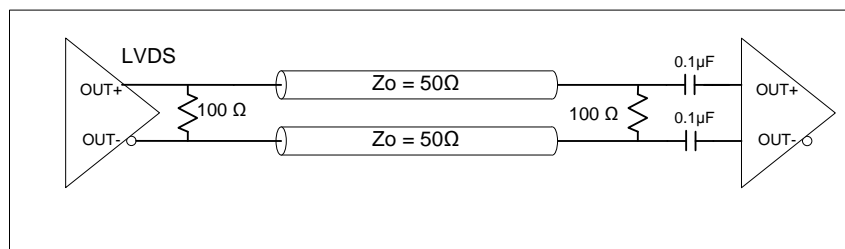


Figure 10. LVDS double AC termination with capacitor close to the load

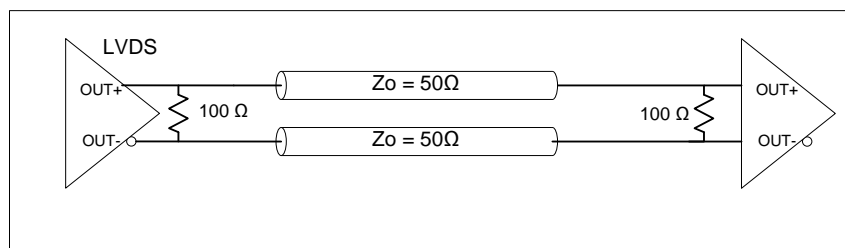


Figure 11. LVDS double DC termination

Termination Diagrams (Continued)

HCSL:

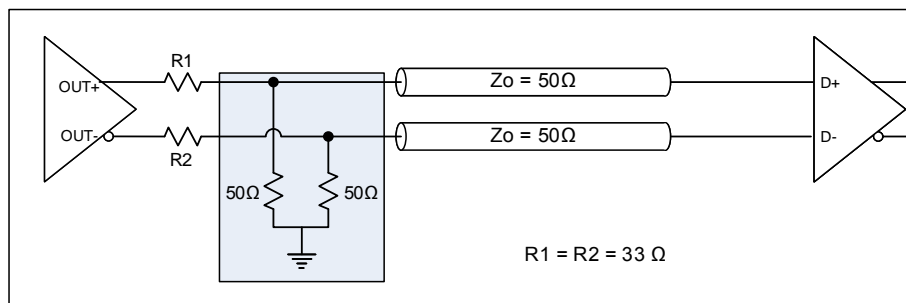


Figure 12. HCSL interface termination

Dimensions and Patterns

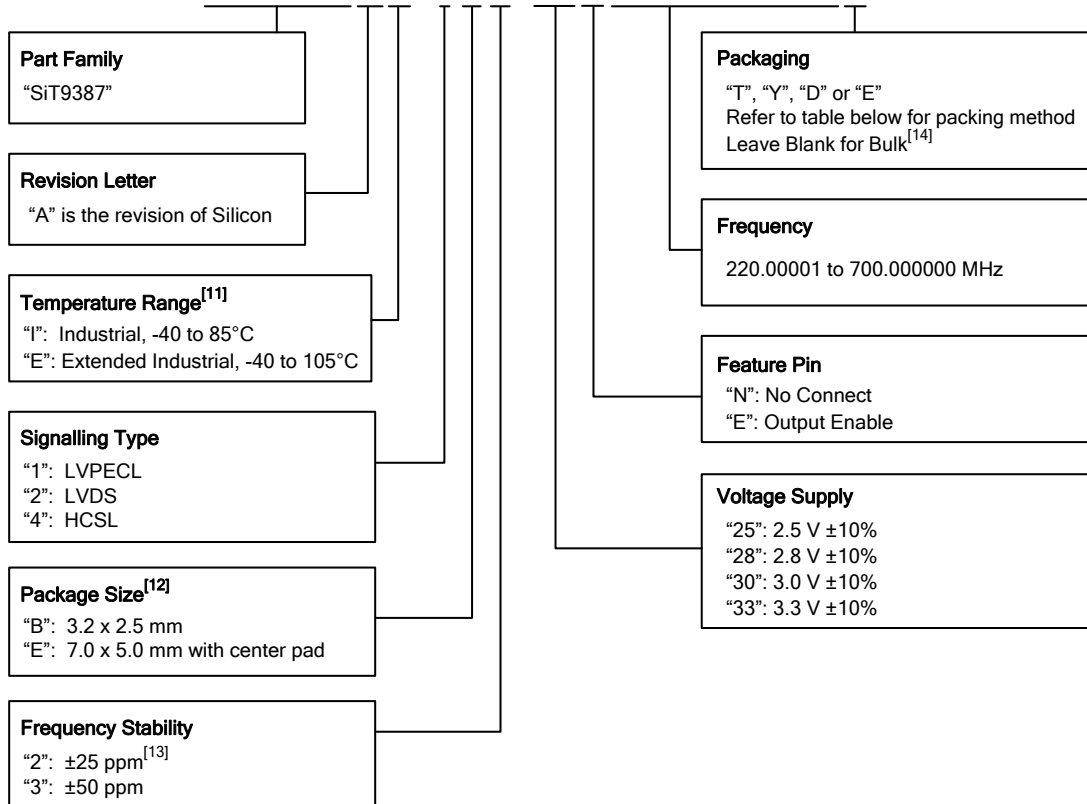
Package Size – Dimensions (Unit: mm) ^[8]	Recommended Land Pattern (Unit: mm) ^[9]																																																									
<p>3.2 x 2.5 x 0.75 mm</p> <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> </div> <div style="width: 45%;"> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th colspan="5">Dimension Table</th> </tr> <tr> <th></th> <th>Symbol</th> <th>Min</th> <th>Nom</th> <th>Max</th> </tr> </thead> <tbody> <tr> <td>TOTAL THICKNESS</td> <td>A</td> <td>0.800</td> <td>0.850</td> <td>0.900</td> </tr> <tr> <td rowspan="2">BODY SIZE</td> <td>X</td> <td>D</td> <td>2.400</td> <td>2.500</td> <td>2.600</td> </tr> <tr> <td>Y</td> <td>E</td> <td>3.200</td> <td>3.200</td> <td>3.300</td> </tr> <tr> <td>LEAD PITCH</td> <td>e</td> <td colspan="3">1.100 BSC</td> </tr> <tr> <td>LEAD LENGTH</td> <td>L</td> <td>0.650</td> <td>0.700</td> <td>0.750</td> </tr> <tr> <td>LEAD WIDTH</td> <td>W</td> <td>0.550</td> <td>0.600</td> <td>0.650</td> </tr> </tbody> </table> </div> </div> <div style="margin-top: 10px; display: flex; justify-content: space-between;"> <div style="width: 45%;"> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="font-size: small;">6L QFN</td> <td style="font-size: small;">Package Outline</td> </tr> <tr> <td style="font-size: small;">3.2 x 2.5 x 0.75 mm</td> <td rowspan="2" style="text-align: center;"></td> </tr> <tr> <td style="font-size: small;">POD-38 Rev A</td> </tr> </table> </div> <div style="width: 45%;"></div> </div>	Dimension Table						Symbol	Min	Nom	Max	TOTAL THICKNESS	A	0.800	0.850	0.900	BODY SIZE	X	D	2.400	2.500	2.600	Y	E	3.200	3.200	3.300	LEAD PITCH	e	1.100 BSC			LEAD LENGTH	L	0.650	0.700	0.750	LEAD WIDTH	W	0.550	0.600	0.650	6L QFN	Package Outline	3.2 x 2.5 x 0.75 mm		POD-38 Rev A	<p>3.2 x 2.5 x 0.75 mm</p>											
Dimension Table																																																										
	Symbol	Min	Nom	Max																																																						
TOTAL THICKNESS	A	0.800	0.850	0.900																																																						
BODY SIZE	X	D	2.400	2.500	2.600																																																					
	Y	E	3.200	3.200	3.300																																																					
LEAD PITCH	e	1.100 BSC																																																								
LEAD LENGTH	L	0.650	0.700	0.750																																																						
LEAD WIDTH	W	0.550	0.600	0.650																																																						
6L QFN	Package Outline																																																									
3.2 x 2.5 x 0.75 mm																																																										
POD-38 Rev A																																																										
<p>7.0 x 5.0 x 0.90 mm^[10]</p> <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> </div> <div style="width: 45%;"> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th colspan="5">Dimension Table</th> </tr> <tr> <th></th> <th>Symbol</th> <th>Min</th> <th>Nom</th> <th>Max</th> </tr> </thead> <tbody> <tr> <td>TOTAL THICKNESS</td> <td>A</td> <td>0.800</td> <td>0.850</td> <td>0.900</td> </tr> <tr> <td rowspan="2">BODY SIZE</td> <td>X</td> <td>D</td> <td>4.900</td> <td>5.000</td> <td>5.100</td> </tr> <tr> <td>Y</td> <td>E</td> <td>6.900</td> <td>7.000</td> <td>7.100</td> </tr> <tr> <td rowspan="2">EP SIZE</td> <td>X</td> <td>J</td> <td>1.400</td> <td>1.500</td> <td>1.600</td> </tr> <tr> <td>Y</td> <td>K</td> <td>3.400</td> <td>3.500</td> <td>3.600</td> </tr> <tr> <td>LEAD PITCH</td> <td>e</td> <td colspan="3">2.540 BSC</td> </tr> <tr> <td>LEAD LENGTH</td> <td>L</td> <td>0.850</td> <td>0.900</td> <td>0.950</td> </tr> <tr> <td>LEAD WIDTH</td> <td>W</td> <td>1.350</td> <td>1.400</td> <td>1.450</td> </tr> </tbody> </table> </div> </div> <div style="margin-top: 10px; display: flex; justify-content: space-between;"> <div style="width: 45%;"> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="font-size: small;">6L QFN</td> <td style="font-size: small;">Package Outline</td> </tr> <tr> <td style="font-size: small;">7.0 x 5.0 x 0.90 mm</td> <td rowspan="2" style="text-align: center;"></td> </tr> <tr> <td style="font-size: small;">POD-37 Rev A</td> </tr> </table> </div> <div style="width: 45%;"></div> </div>	Dimension Table						Symbol	Min	Nom	Max	TOTAL THICKNESS	A	0.800	0.850	0.900	BODY SIZE	X	D	4.900	5.000	5.100	Y	E	6.900	7.000	7.100	EP SIZE	X	J	1.400	1.500	1.600	Y	K	3.400	3.500	3.600	LEAD PITCH	e	2.540 BSC			LEAD LENGTH	L	0.850	0.900	0.950	LEAD WIDTH	W	1.350	1.400	1.450	6L QFN	Package Outline	7.0 x 5.0 x 0.90 mm		POD-37 Rev A	<p>7.0 x 5.0 x 0.90 mm^[10]</p> <p>Note: Circles in center pad are thermal vias, recommended to improve thermal performance</p>
Dimension Table																																																										
	Symbol	Min	Nom	Max																																																						
TOTAL THICKNESS	A	0.800	0.850	0.900																																																						
BODY SIZE	X	D	4.900	5.000	5.100																																																					
	Y	E	6.900	7.000	7.100																																																					
EP SIZE	X	J	1.400	1.500	1.600																																																					
	Y	K	3.400	3.500	3.600																																																					
LEAD PITCH	e	2.540 BSC																																																								
LEAD LENGTH	L	0.850	0.900	0.950																																																						
LEAD WIDTH	W	1.350	1.400	1.450																																																						
6L QFN	Package Outline																																																									
7.0 x 5.0 x 0.90 mm																																																										
POD-37 Rev A																																																										

Notes:

8. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
9. A capacitor of value 0.1 μF or higher between Vdd and GND is required. An additional 10 μF capacitor between Vdd and GND is required for the best phase jitter performance
10. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

Ordering Information

SiT9387AC-1B2-33E 322.265625T



Notes:

- 11. Contact [SiTime](#) for higher temperature range options
- 12. Contact [SiTime](#) for 5.0 x 3.2 mm package
- 13. Contact [SiTime](#) for ±25 ppm option
- 14. Bulk is available for sampling only

Table 10. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0	—	—	—	—	T	Y
3.2 x 2.5	D	E	T	Y	—	—

Table 11 .Revision History

Revision	Release Date	Change Summary
0.90	11/24/2017	Initial release

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | Phone: +1-408-328-4400 | Fax: +1-408-328-4439

© SiTime Corporation 2017. The information contained herein is subject to change at any time without notice. SiTime assumes no responsibility or liability for any loss, damage or defect of a Product which is caused in whole or in part by (i) use of any circuitry other than circuitry embodied in a SiTime product, (ii) misuse or abuse including static discharge, neglect or accident, (iii) unauthorized modification or repairs which have been soldered or altered during assembly and are not capable of being tested by SiTime under its normal test conditions, or (iv) improper installation, storage, handling, warehousing or transportation, or (v) being subjected to unusual physical, thermal, or electrical stress.

Disclaimer: SiTime makes no warranty of any kind, express or implied, with regard to this material, and specifically disclaims any and all express or implied warranties, either in fact or by operation of law, statutory or otherwise, including the implied warranties of merchantability and fitness for use or a particular purpose, and any implied warranty arising from course of dealing or usage of trade, as well as any common-law duties relating to accuracy or lack of negligence, with respect to this material, any SiTime product and any product documentation. Products sold by SiTime are not suitable or intended to be used in a life support application or component, to operate nuclear facilities, or in other mission critical applications where human life may be involved or at stake. All sales are made conditioned upon compliance with the critical uses policy set forth below.

CRITICAL USE EXCLUSION POLICY

BUYER AGREES NOT TO USE SITIME'S PRODUCTS FOR ANY APPLICATION OR IN ANY COMPONENTS USED IN LIFE SUPPORT DEVICES OR TO OPERATE NUCLEAR FACILITIES OR FOR USE IN OTHER MISSION-CRITICAL APPLICATIONS OR COMPONENTS WHERE HUMAN LIFE OR PROPERTY MAY BE AT STAKE.

SiTime owns all rights, title and interest to the intellectual property related to SiTime's products, including any software, firmware, copyright, patent, or trademark. The sale of SiTime products does not convey or imply any license under patent or other rights. SiTime retains the copyright and trademark rights in all documents, catalogs and plans supplied pursuant to or ancillary to the sale of products or services by SiTime. Unless otherwise agreed to in writing by SiTime, any reproduction, modification, translation, compilation, or representation of this material shall be strictly prohibited.