SiT1534

Ultra-Small, Ultra-Low Power 1 Hz – 32.768 kHz Programmable Oscillator

Features

- Factory programmable from 32.768 kHz down to 1 Hz
- <20 ppm frequency tolerance
- Smallest footprint in chip-scale (CSP): 1.5 x 0.8 mm
- Pin-compatible to 2.0 x 1.2 mm XTAL SMD package
- Ultra-low power: <1 µA
- Vdd supply range: 1.5 V to 3.63 V over -55°C to +85°C
- Supports low-voltage battery backup from a coin cell or supercap
- Oscillator output eliminates external load caps
- Internal filtering eliminates external Vdd bypass cap
- NanoDrive™ programmable output swing for lowest power
- Pb-free, RoHS and REACH compliant
- PFAS free option available with ordering code 'P'

Applications

- Mobile Phones
- Tablets
- Health and Wellness Monitors
- Fitness Watches
- Sport Video Cams
- Wireless Keypads
- Ultra-Small Notebook PC
- Pulse-per-Second (pps) Timekeeping
- RTC Reference Clock
- Battery Management Timekeeping

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Electrical Specifications

Table 1. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Programmable Output Frequency		1.00		32768.0	Hz	Factory programmed between 1 and 32.768 kHz in powers of 2
Frequency Stability						
Frequency Tolerance[1]	F_tol			20	ppm	T_A = 25°C, post reflow, includes underfill, Vdd: 1.5 V – 3.63 V
Frequency Stability[2]	F_stab			75	ppm	T_A = -10°C to +70°C, Vdd: 1.5 V – 3.63 V
				100		T_A = -40°C to +85°C, Vdd: 1.5 V – 3.63 V
				150		T_A = -55°C to +85°C, Vdd: 1.5 V – 3.63 V
				250		T_A = -10°C to +70°C, Vdd: 1.2 V – 1.5 V
25°C Aging		-1		1	ppm	1st Year
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.2		3.63	V	T_A = -10°C to +70°C
		1.5		3.63	V	T_A = -55°C to +85°C
Core Operating Current[3]	Idd		0.9		µA	T_A = 25°C, Vdd: 1.8 V. No load
				1.3		T_A = -10°C to +70°C, Vdd max: 3.63 V. No load
				1.4		T_A = -55°C to +85°C, Vdd max: 3.63 V. No load
Output Stage Operating Current[3]	Idd_out		0.065	0.125	µA/Vpp	T_A = -40°C to +85°C, Vdd: 1.5 V – 3.63 V. No load
Power-Supply Ramp	t_Vdd Ramp			100	ms	Over temperature, 0 to 90%
Start-up Time[4]	t_start			300 + 1 period	ms	T_A = 25°C ±10°C, valid output
				500 + 1 period		T_A = -55°C to +85°C, valid output
Operating Temperature Range						
Commercial Temperature	T_use	-10		70	°C	
Industrial Temperature		-40		85	°C	
Extended Cold Industrial Temperature		-55		85	°C	

Notes:

1. Measured peak-to-peak. Tested with Agilent 53132A frequency counter. Due to the low operating frequency, the gate time must be ≥100 ms to ensure an accurate frequency measurement.
2. Measured peak-to-peak. Inclusive of Initial Tolerance at 25°C, and variations over operating temperature, rated power supply voltage and load. Stability is specified for two operating voltage ranges. Stability progressively degrades with supply voltage below 1.5 V.
3. Core operating current does not include output driver operating current or load current. To derive total operating current (no load), add core operating current + (0.065 µA/V) * (output voltage swing).
4. Measured from the time Vdd reaches 1.5 V.

Table 1. Electrical Characteristics (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVCMOS Output Option, T_A = -55°C to +85°C, typical value is T_A = 25°C						
Output Rise/Fall Time	tr, tf		100	200	ns	10-90% (Vdd), 15 pF load, Vdd = 1.5 V to 3.63 V
Output Clock Duty Cycle	DC	48		52	%	
Output Voltage High	VOH	90%			V	Vdd: 1.5 V – 3.63 V. I_{OH} = -10 µA, 15 pF
Output Voltage Low	VOL			10%	V	Vdd: 1.5 V – 3.63 V. I_{OL} = 10 µA, 15 pF
NanoDrive™ Programmable, Reduced Swing Output						
Output Rise/Fall Time	tf, tf			200	ns	30-70% (V_{OL}/V_{OH}), 10 pF Load
Output Clock Duty Cycle	DC	48		52	%	
AC-coupled Programmable Output Swing	V_sw		0.20 to 0.80		V	SiT1534 does not internally AC-couple. This output description is intended for a receiver that is AC-coupled. See Table 6 for acceptable NanoDrive swing options Vdd: 1.5 V – 3.63 V, 10 pF Load, I_{OH} / I_{OL} = ±0.2 µA.
DC-Biased Programmable Output Voltage High Range	VOH		0.60 to 1.225		V	Vdd: 1.5 V – 3.63 V. I_{OH} = -0.2 µA, 10 pF Load. See Table 5 for acceptable VOH/VOL setting levels
DC-Biased Programmable Output Voltage Low Range	VOL		0.35 to 0.80		V	Vdd: 1.5 V – 3.63 V. I_{OL} = 0.2 µA, 10 pF Load. See Table 5 for acceptable V_{OH}/V_{OL} setting levels
Programmable Output Voltage Swing Tolerance		-0.055		0.055	V	T_A = -40°C to +85°C, Vdd = 1.5 V to 3.63 V
Jitter Performance						
Period Jitter	T_djitt		35		ns_{RMS}	Cycles = 10,000, T_A = 25°C, Vdd = 1.5 V – 3.63 V

Table 2. Pin Configuration (SMD)

Pin	Symbol	I/O	Functionality
1	NC	No Connect, don't care	No Connect. Will not respond to any input signal. When the SiT1534 is used as an alternative to an XTAL, this pin is typically connected to the receiving ICs X Out pin. In this case, the SiT1534 will not be affected by the signal on this pin.
2	GND	Power Supply Ground	Connect to ground.
3	CLK Out	OUT	Oscillator clock output. When the SiT1534 is used as an alternative to an XTAL, the CLK Out is typically connected to the receiving ICs X IN pin. No need for load capacitors. The output driver is independent of capacitive loading.
4	Vdd	Power Supply	Connect to power supply 1.2 V ≤ Vdd ≤ 3.63 V. Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). For more information about the internal power-supply filtering, see the Power Supply Noise Immunity section in the detailed description. Contact SiTime for applications that require a wider operating supply voltage range.

SMD Package (Top View)

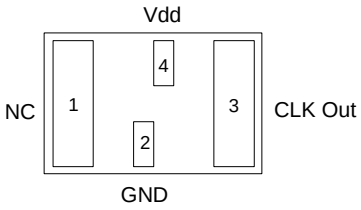


Figure 1. Pin Assignments (SMD)

Table 3. Pin Configuration (CSP)

Pin	Symbol	I/O	Functionality
1, 4	GND	Power Supply Ground	Connect to ground. Acceptable to connect pin 1 and 4 together. Both pins must be connected to GND.
2	CLK Out	OUT	Oscillator clock output. The CLK can drive into a Ref CLK input or into an ASIC or chip-set's 32kHz XTAL input. When driving into an ASIC or chip-set oscillator input (X IN and X Out), the CLK Out is typically connected directly to the XTAL IN pin. No need for load capacitors. The output driver is intended to be insensitive to capacitive loading.
3	Vdd	Power Supply	Connect to power supply 1.2 V ≤ Vdd ≤ 3.63 V. Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). For more information about the internal power-supply filtering, see the Power Supply Noise Immunity section in the detailed description. Contact SiTime for applications that require a wider operating supply voltage range.

CSP Package (Top View)

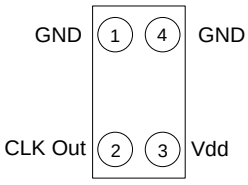


Figure 2. Pin Assignments (CSP)

System Block Diagram

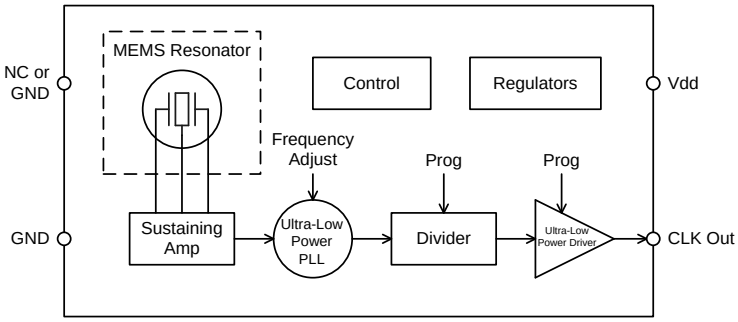


Figure 3. SiT1534 Block Diagram

Table 4. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Condition	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 3.63	V
Short Duration Maximum Power Supply Voltage (Vdd)	≤30 minutes	4.0	V
Continuous Maximum Operating Temperature Range	Vdd = 1.5 V - 3.63 V	105	°C
Short Duration Maximum Operating Temperature Range	Vdd = 1.5 V - 3.63 V, ≤30 mins	125	°C
Maximum Continuous Operating Life at Temperature Extreme (meeting datasheet limits)	T_A = -55°C, Continuous Vdd = 1.8 V – 3.3 V ±10%	8	Hours
Human Body Model (HBM) ESD Protection	JESD22-A114	3000	V
Charge-Device Model (CDM) ESD Protection	JESD22-C101	750	V
Machine Model (MM) ESD Protection	JESD22-A115	300	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	10,000	g
Mechanical Vibration Resistance	Mil 883, Method 2007	70	g
2012 SMD Junction Temperature		150	°C
1508 CSP Junction Temperature		150	°C
Storage Temperature		-65°C to 150°C	

Description

The SiT1534 is the first programmable oscillator capable of a frequency range between 32.768 kHz down to 1 Hz for true pulse-per-second (PPS) operation. SiTime's silicon MEMS technology enables the smallest footprint and chip-scale packaging. In the chip-scale package (CSP), these devices reduce footprint by as much as 80% compared to existing 2.0 x 1.2 mm SMD XTAL packages. Unlike XTALs, the SiT1534 oscillator output enables greater component placement flexibility and eliminates external load capacitors, thus saving additional component count and board space. And unlike standard oscillators, the SiT1534 features NanoDrive™, a factory programmable output that reduces the voltage swing to minimize power.

SiTime's MEMS oscillators consist of MEMS resonators and a programmable analog circuit. Our MEMS resonators are built with SiTime's unique MEMS First® process. A key manufacturing step is EpiSeal® during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, SiTime's MEMS resonator die can be used like any other semiconductor die. One unique result of SiTime's MEMS First and EpiSeal manufacturing processes is the capability to integrate SiTime's MEMS die with a SOC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cheaper solution to the customer.

For applications that require XTAL resonator compatibility, the SiT1534 is available in the 2.0 x 1.2 mm (2012) package. Unlike XTAL resonators, SiTime's silicon MEMS oscillators require a power supply (Vdd) and ground (GND) pin. Vdd and GND pins are conveniently placed between the two large XTAL pins. When using the SiTime Solder Pad Layout (SPL), the SiT1534 footprint is compatible with existing 32 kHz XTALs in the 2012 SMD package. Figure 4 shows the comparison between the quartz XTAL footprint and the SiTime footprint.

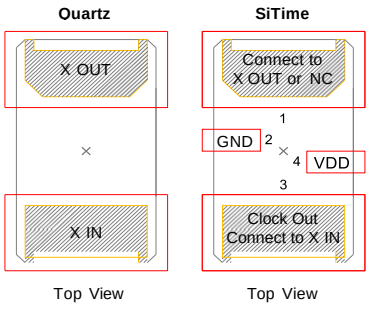


Figure 4. SiT1534 Footprint Compatibility with Quartz XTAL Footprint[5]

Frequency Stability

The SiT1534 is factory calibrated (trimmed) to guarantee frequency stability to be less than 20 ppm at room temperature and less than 100 ppm over the full -40°C to +85°C temperature range. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point, the SiT1534 temperature coefficient is extremely flat across temperature. This device maintains less than 100 ppm frequency stability over the full operating temperature range when the operating voltage is between 1.5 and 3.63 V as shown in Figure 5.

Functionality is guaranteed over the full supply voltage range. However, frequency stability degrades below 1.5 V and steadily degrades as it approaches 1.2 V due to the internal regulator limitations.

When measuring the SiT1534 output frequency with a frequency counter, it is important to make sure the counter's gate time is ≥100 ms. The slow frequency of a 32 kHz clock will give false readings with faster gate times.

For applications that require a higher operating voltage range, consider the SiT1544 with a 2.7 V to 4.5 V supply voltage range.

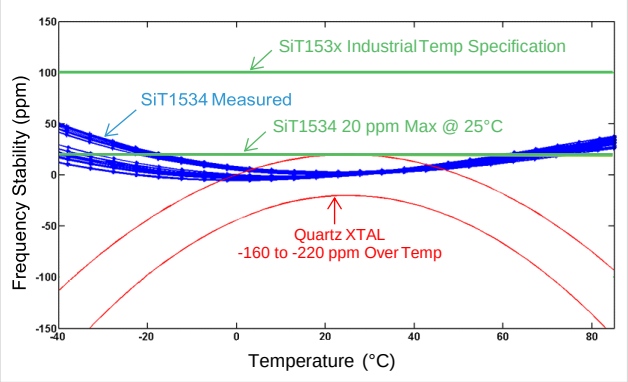


Figure 5. SiTime vs. Quartz

Note:

5. On the SiTime device, X IN is not internally connected and will not respond to any signal. It is acceptable to connect to chipset X OUT.

Power Supply Noise Immunity

In addition to eliminating external output load capacitors common with standard XTALs, this device includes special power supply filtering and thus, eliminates the need for an external Vdd bypass-decoupling capacitor. This feature further simplifies the design and keeps the footprint as small as possible. Internal power supply filtering is designed to reject AC-noise greater than ±150 mVpp and beyond 10 MHz frequency components.

Programmable Frequency

The SiT1534 is the first oscillator to feature a programmable frequency range between 1 Hz and 32.768 kHz in powers of two. Reducing the frequency significantly reduces the output load current (C*V*F). For example, reducing the frequency from 32.768 kHz to 10 kHz improves load current by 70%. Similarly, reducing the output frequency from 32.768 kHz down to 1 Hz reduces the load current by more than 99%.

The Part Number Ordering shows the specific frequency options.

NanoDrive™ Reduced Swing Output Voltage

For low-power applications that drive directly into a chip-set's XTAL input, the reduced swing output is ideal. SiTime's unique NanoDrive™, factory-programmable output stage is optimized for low voltage swing to minimize power and maintain compatibility with the downstream oscillator input (X IN pin). The SiT1534 output swing is factory programmed between 250 mV and 800 mV. For DC-coupled applications, output V_{OH} and V_{OL} are individually factory programmed. Contact SiTime for programming support.

Power-up

The SiT1534 starts-up to a valid output frequency within 300 ms when operating at 32.768 kHz. For frequencies less than 32.768 kHz, the start-up time can increase by an additional clock period. The maximum start-up time over temperature is 500 ms max over temperature plus a clock period. For example, the maximum start-up time for a 256 Hz clock is 500 ms + 3.9 ms. To ensure the device starts-up within the specified limit, make sure the power-supply ramps-up in approximately 10 – 20 ms (to within 90% of Vdd). Start-up time is measured from the time Vdd reaches 1.5 V. For applications that require start-up between 1.2 V and 1.5 V, the start-up time will be typically 50 ms longer.

SiT1534 NanoDrive™

Figure 6 shows a typical output waveform of the SiT1534 (into a 10 pF load) when factory programmed for a 0.70 V swing and DC bias (V_{OH}/V_{OL}) for 1.8 V logic:

Example:

- NanoDrive™ part number coding: **D14**.
  Example part number: SiT1534AI-J4-**D14**-32.768
- V_{OH} = 1.1 V, V_{OL} = 0.4 V (V_{SW} = 0.70 V)

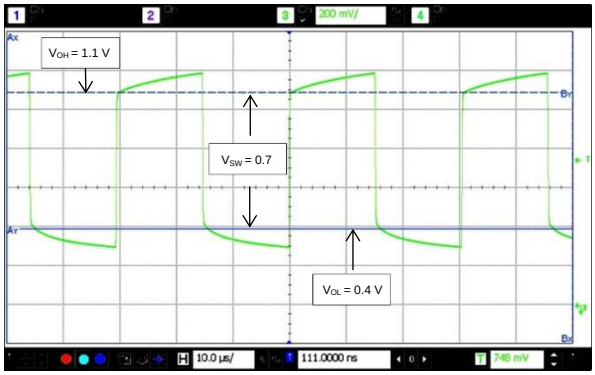


Figure 6. SiT1534AI-J4-D14-32.768 Output Waveform (10 pF load)

Table 5 shows the supported NanoDrive™ V_{OH}, V_{OL} factory programming options.

Table 5. Acceptable V_{OH}/V_{OL} NanoDrive™ Levels

NanoDrive	V_{OH} (V)	V_{OL} (V)	Swing (mV)	Comments
D26	1.2	0.6	600 ±55	1.8 V logic compatible
D14	1.1	0.4	700 ±55	1.8 V logic compatible
D74	0.7	0.4	300 ±55	XTAL compatible
AA3	n/a	n/a	300 ±55	XTAL compatible

SiT1534 Full Swing LVCMOS Output

The SiT1534 can be factory programmed to generate full-swing LVCMOS levels. Figure 5 shows the typical waveform (Vdd = 1.8 V) at room temperature into a 15 pF load.

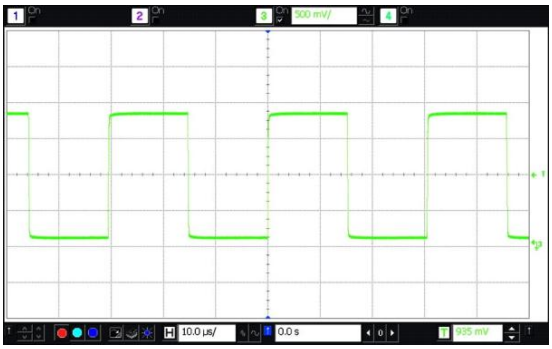


Figure 7. LVCMOS Waveform (Vdd = 1.8 V) into 15 pF Load

Example:

- LVCMOS output part number coding is always **DCC**
  Example part number: SiT1534AI-J4-**DCC**-32.768

Calculating Load Current

No Load Supply Current

When calculating no-load power for the SiT1534, the core and output driver components need to be added. Since the output voltage swing can be programmed for reduced swing between 250 mV and 800 mV for ultra-low power applications, the output driver current is variable and is a function of the output voltage swing and the output frequency. Therefore, no-load operating supply current is broken into two sections; core and output driver. The real benefit of NanoDrive™ is shown in the Total Supply Current with Load calculation in the next section. The equation is as follows:

Total Supply Current (no load) = Idd Core + Idd Output Driver

Example 1: Full-swing LVCMOS

- Vdd = 1.8 V
- Fout = 32.768 kHz
- Vout = Vdd
- Idd Output Driver: (3.5 pF)(Vout)(Fout) = 206 nA
- Idd Core = 900 nA (typ)
- Vout = Vdd = 1.8 V

Supply Current = 900 nA + 206 nA = 1.1 µA

Example 2: NanoDrive™ Reduced Swing

- Vdd = 1.8 V
- Fout = 32.768 kHz
- Vout (programmable) = Voh – Vol = 1.1 V - 0.6 V = 500 mV
- Idd Core = 900 nA (typ)
- Idd Output Driver: (3.5 pF)(Vout)(Fout) = 57 nA

Supply Current = 900 nA + 57 nA = 957 nA

Calculating Total Supply Current with Load

To calculate the total supply current, including the load, follow the equation listed below. Note the 35% reduction in power with NanoDrive™ as shown in Example 2. Reducing the output clock frequency reduces the load current significantly, as shown in Example 3.

Total Current = Idd Core + Idd Output Driver + Load Current

Example 1: Full-swing LVCMOS

- Vdd = 1.8 V
- Fout = 32.768 kHz
- Vout = Vdd
- Idd Core = 900 nA
- Idd Output Driver: (3.5 pF)(Vout)(Fout) = 206 nA
- Load Current: (10 pF)(1.8 V)(32.768 kHz) = 590 nA

Total Current with Load = 900 nA + 205 nA + 590 nA =1.5 µA

Example 2: NanoDrive™ Reduced Swing

- Vdd = 1.8 V
- Fout = 32.768 kHz
- Idd Core = 900 nA
- Vout (programmable): Voh – Vol = 1.2 V - 0.6 V = 600 mV
- Idd Output Driver: (3.5 pF)(Vout)(Fout) = 69 nA
- Load Current: (5 pF)(0.6 V)(32.768 kHz) = 98 nA

Total Current with Load = 900 nA + 69 nA + 98 nA = 1.07 µA

Example 3: LVCMOS and 1 Hz Output Frequency

- Same conditions as above example 1, but with output frequency = 1 Hz. This will significantly reduce the current consumption from the output stage and the load.
- Idd Core = 900 nA
- Idd Output Stage = (3.5 pF)(1.8 V)(1 Hz) = 6.3 pA
- 1 Hz Output Frequency impacts the load current as shown below:

  Load Current = CVF = (10 pF)(1.8 V)(1 Hz) = 18 pA

Total Supply Current with Load = Core Current + Output Stage Current + Load Current = 900 nA + 0.0063 nA + 0.018 nA = 900 nA

Summary: Reducing the output frequency to 1 Hz virtually eliminates the current consumption from the output stage and load current.

Typical Operating Curves

(T_A = 25°C, Vdd = 1.8 V, unless otherwise stated)

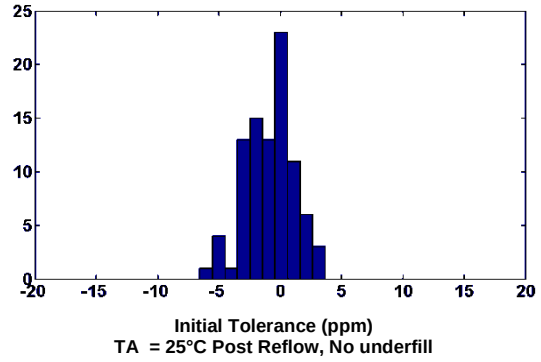


Figure 8. Initial Tolerance Histogram

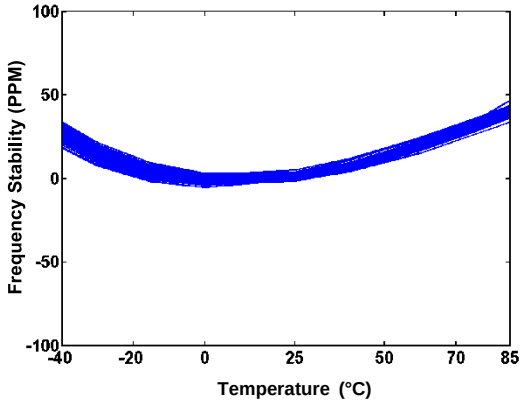


Figure 9. Frequency Stability over Temperature

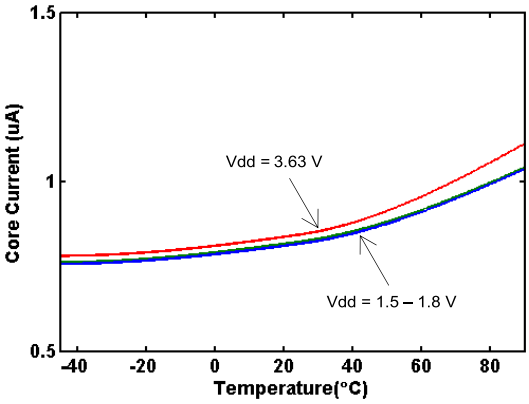


Figure 10. Core Current over Temperature

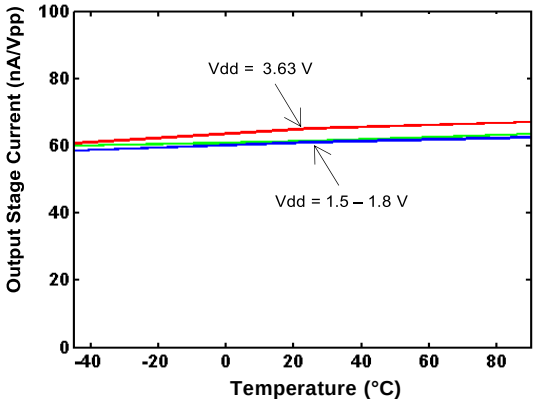


Figure 11. Output Stage Current over Temperature

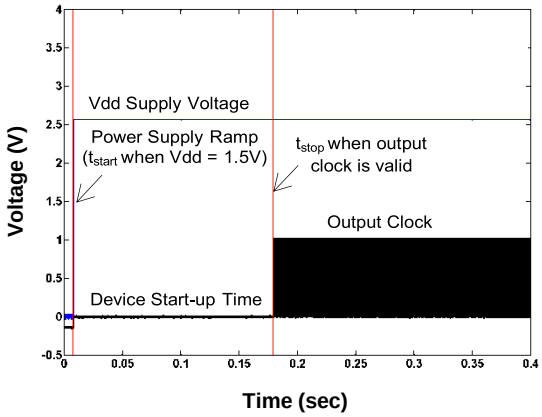


Figure 12. 32.768 kHz Start-up Time

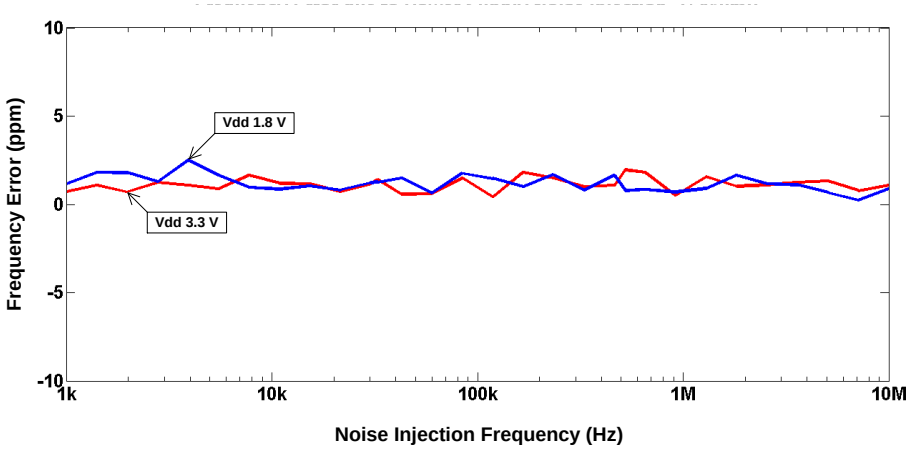


Figure 13. Power Supply Noise Rejection
(±150 mV Noise)

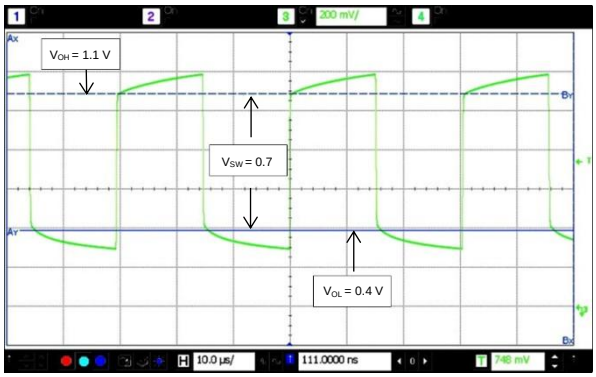


Figure 14. NanoDrive™ Output Waveform
(V_{OH} = 1.1 V, V_{OL} = 0.4 V; SiT1534AI-J4-D14-32.768)

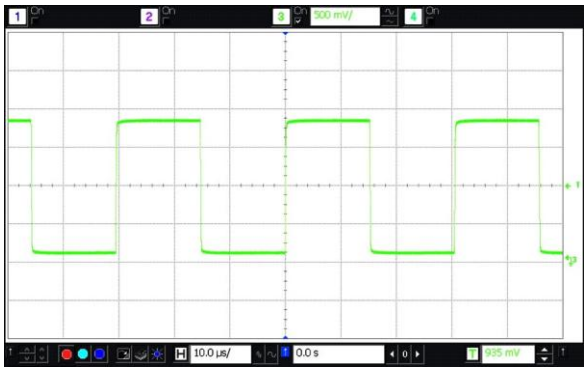
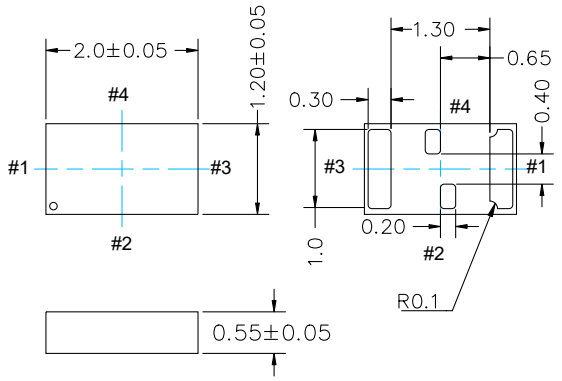
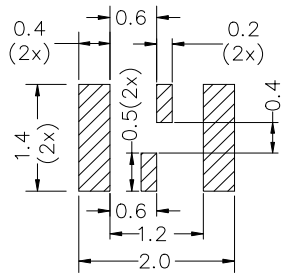


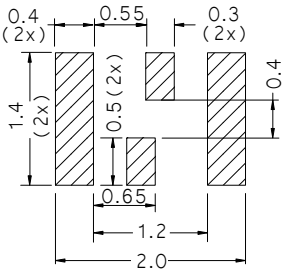
Figure 15. LVCMOS Output Waveform
(V_{swing} = 1.8 V, SiT1534AI-J4-DCC-32.768)

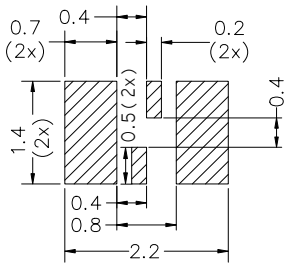
Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[6]	Recommended Land Pattern (Unit: mm)
2.0 x 1.2 mm SMD	**SiTime Only SPL**
	SiTime Alternate SPL with Larger Center Pads
	XTAL Compatible SPL







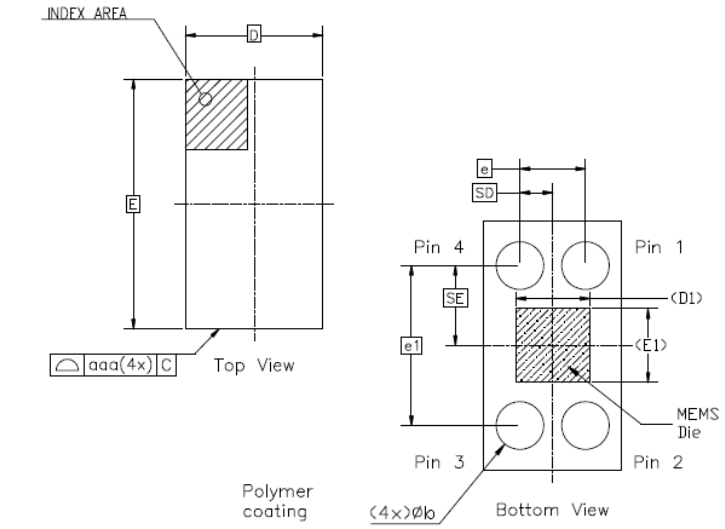


Note:

6. For marking guidance, see SiTime Manufacturing Notes in the Quality & Reliability section.

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)



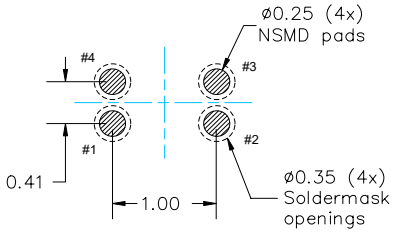
Dimension Table (mm)				
Item		SYMBOL	MINIMUM	NOMINAL	MAXIMUM
Total Thickness		A	0.48	0.54	0.60
Stand Off		A1	0.22		0.28
MEMS Clearance		A2	0.027		0.113
Film Thickness		A3	0.036	0.040	0.044
Wafer Thickness		A4	0.225	0.250	0.275
Ball Diameter		b	0.30	0.315	0.33
Ball Pitch	X	e	0.41 BSC		
	Y	e1	1.00 BSC		
MEMS	X	D1	0.46 REF		
	Y	E1	0.46 REF		
Body Size	X	D	0.84 BSC		
	Y	E	1.54 BSC		
Ball To Center	X	SD	0.205 BSC		
	Y	SE	0.500 BSC		
Package Edge Tolerance		aaa	0.040		
Coplanarity		ccc	0.075		

4 LD – 1.5 x 0.8 x 0.55 mm

Package Outline

POD-35 Rev A

Recommended Land Pattern (Unit: mm)



(soldermask openings shown with dashed line around NSMD pad)

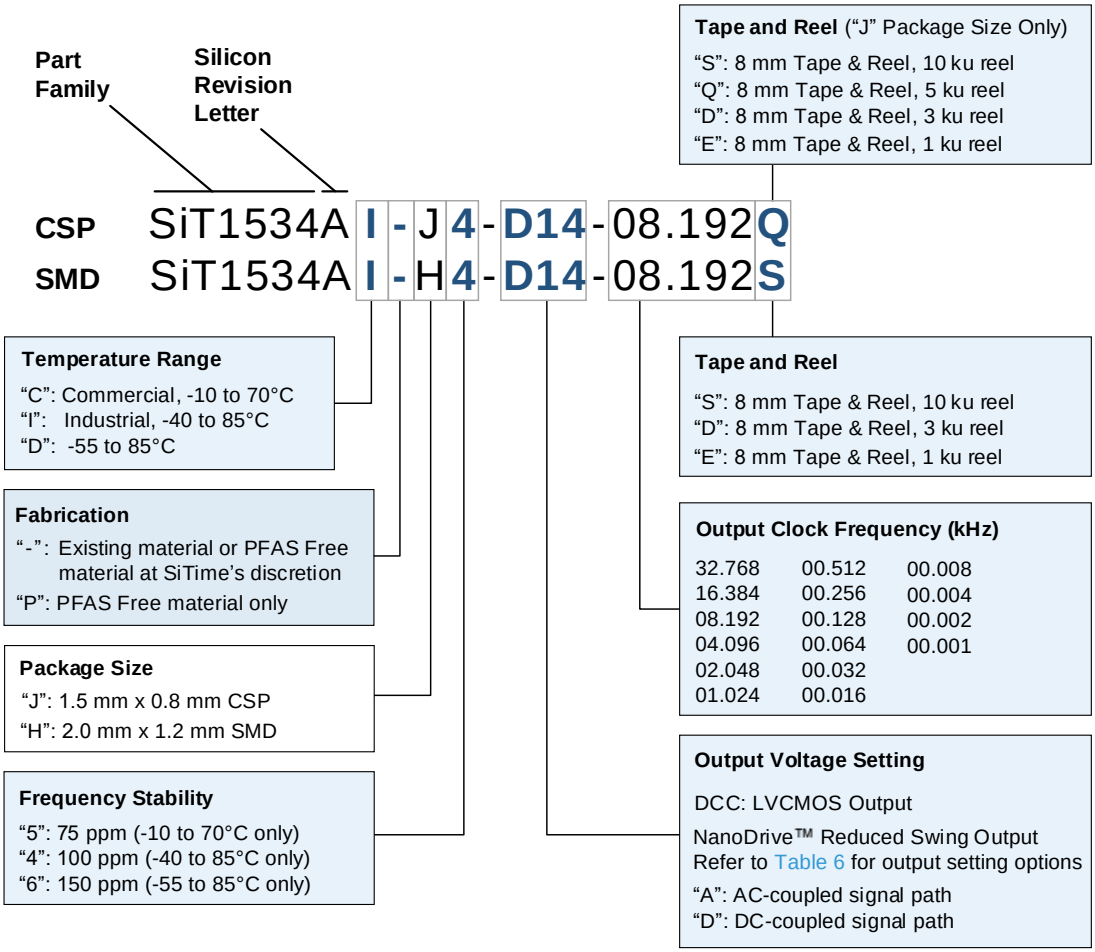
Recommended 4-mil (0.1mm) stencil thickness

Manufacturing Guidelines

1) No Ultrasonic Cleaning: Do not subject the SiT1534 to an ultrasonic cleaning environment. Permanent damage or long term reliability issues to the MEMS structure may occur.
2) Applying board-level underfill (BLUF) to the device is acceptable. It is reasonable to expect a slight shift in the frequency and has been accounted for in the frequency tolerance specification. Tested with UF3810, UF3808, and FP4530 underfill.
3) CSP Reflow profile, per JESD22-A113D.
4) When designing-in the SiT1534 in the 2012 SMD package into noisy, high EM environments, we recommend the following design guidelines:
    - Place oscillator as far away from EM noise sources as possible (e.g., high-voltage switching regulators, motor drive control).
    - Route noisy PCB traces, such as digital data lines or high di/dt power supply lines, away from the SiTime oscillator.
    - Add a low ESR/ESL, 0.1 uF to 1.0 uF ceramic capacitor (X7R) to help filter high frequency noise on the Vdd power-supply line. Place it as close to the SiTime oscillator Vdd pin as possible.
    - Place a solid GND plane underneath the SiTime oscillator to shield the oscillator from noisy traces on the other board layers.
    - For details, please refer to the PCB Layout Guidelines in AN10006.
5) For additional manufacturing guidelines and marking/ tape-reel instructions, refer to SiTime Manufacturing Notes.

Ordering Information

Part number characters in blue represent the customer specific options. The other characters in the part number are fixed.



The following examples illustrate how to select the appropriate temp range and output voltage requirements:

Example 1: SiT1534AI-J4-D14-08.192

1) Industrial temp & corresponding 100 ppm frequency stability
2) Output swing requirements:
   a) Output frequency = 8.192 kHz
   b) “D” = DC-coupled receiver
   c) “1” = V_{OH} = 1.1 V
   d) “4” = V_{OL} = 0.4 V

Example 2: SiT1534AC-J5-AA3-00.001

1) Commercial temp & corresponding 75 ppm frequency stability
2) Output swing requirements:
   a) Output frequency = 1 Hz
   b) “A” = AC-coupled receiver
   c) “A” = AC-coupled receiver
   d) “3” = 300 mV swing

Table 6. Acceptable V_{OH}/V_{OL} NanoDrive™ Levels[7]

NanoDrive	V_{OH} (V)	V_{OL} (V)	Swing (mV)	Comments
D26	1.2	0.6	600 ±55	1.8 V logic compatible
D14	1.1	0.4	700 ±55	1.8 V logic compatible
D74	0.7	0.4	300 ±55	XTAL compatible
AA3	n/a	n/a	300 ±55	XTAL compatible

Note:

7. If these available options do not accommodate your application, contact SiTime for other NanoDrive options.

Table 7. Revision History

Version	Release Date	Change Summary
1.0	3-Sep-2014	Rev 0.9 Preliminary to Rev 1.0 Production Release Added start-up time at T_A = 85°C Added typical operating plots Labeled 25C frequency stability as Frequency Tolerance Added Manufacturing Guidelines section
1.1	25-Nov-2014	Added 2012 SMD package design/mfg guidelines
1.2	5-Jan-2016	Updated NanoDrive options
1.3	3-Apr-2016	Added SiTime alternate landing pattern option Updated Note 6
1.31	18-Jan-2018	Updated SPL, page layout changes
1.4	1-Jun-2018	Added -55 to 85°C temperature range option Updated POD (Package Outline Drawing) Updated logo and company address, other page layout changes
1.41	8-Aug-2023	Formatting, rev table date format, TempFlat MEMS logo and trademarks update Added Q-suffix to the Ordering table as CSP option only Fixed Ordering Example 2; Updated icons links on page 1 with SiTimeDirect availability
1.42	17-Jun-2024	PFAS free Ordering Code update Updated icons links on page 1, updated disclaimer
2.0	6-Apr-2025	Removed preliminary wording for PFAS free from Ordering Information

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